Evolution of the CERN Power Converter Function Generator/Controller for operation in fast cycling accelerators

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FGC1
Development from 1996-1999
Used in LHC Test Facility

Radiation tolerance added → More robust

FGC2
Development from 2000-2005
Used in LHC

Faster, cheaper and smaller → No Radiation Tolerance

FGC3
Development from 2007-2011
Used in PS Booster

FGC3

Motherboard

- MCU + DSP architecture.
- Programmable logic.
- Local terminal via USB.
- I/O Digital signals :
  - TTL 3.3v, 5V
  - Open Collector
  - Interlock Relay
- Serial busses
- 1-wire Dallas identification bus

Ethernet Network Interface

- Ethernet as synchronous fieldbus
- Standard 100Mbps LAN
- 1500 bytes packets
- External 50Hz synchronisation pulse needed

Analogue Interface

- 4 high ADC channels, 50KHz bandwidth
- 2 16bits DAC channels
- Internal +10v, -10v reference for automatic calibration
- Internal bus matrix for channel path selection

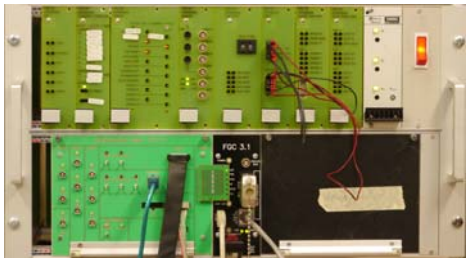
WorldFIP Network Interface

- WorldFIP as synchronous fieldbus
- 1.5Mbps multidrop bus
- 122 bytes packets
- No synchronisation pulse needed

First operational FGC3 in a PS Booster Power Converter

Despite the completely different MCUs, DSPs and fieldbus technologies, the FGC3 is running the software developed for the FGC2. By maintaining the core architecture combined with the flexibility given by the programmable logic and the separation of functionality into different modules, both generations of FGC appear almost identical at the conceptual level.
By inheriting technology from the FGC2, the project saved an estimated 30 FTE years compared to starting from scratch.

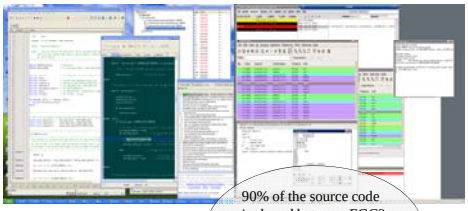
Chassis for applications development and debugging



This chassis allows the simulation of the power converter signals, the connection of debugger interfaces for the 3 processors, the use of test points and measurement of analog signals.

FGC software

Development from 1999-2011



90% of the source code is shared between FGC2 and FGC3.
System applications are the same for both.

The porting and debugging of the low-level functions to the new FGC3 took about 1 year, while for the higher level functions it took another 6 months. By comparison the development of the current operational FGC2 software took twelve years.
As hardware design tools (PCB and FPGA) become more powerful, it has become clear that it is the software which becomes the hardest and most time consuming part of an embedded converter controller development project.

Ethernet Pulse Injector

The required 50Hz synchronisation signal, when using the Ethernet daughter board, is injected in a spare pair of the Ethernet UTP cable by the Pulse Injector Box

Ethernet switch and sync pulse injector